HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

The ULN2001A is a general-purpose array and can be used with TTL and CMOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V PMOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

logic symbol†

logic diagram

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
schematics (each Darlington pair)

- **ULN2001A**
  - 7.2 kΩ
  - 3 kΩ
  - Input B
  - E
  - Output C
  - COM

- **ULN2002A**
  - 7 V
  - 10.5 kΩ
  - 7.2 kΩ
  - 3 kΩ
  - Input B
  - E
  - Output C
  - COM

- **ULN2003A, ULN2004A**
  - 7.2 kΩ
  - 3 kΩ
  - Input B
  - R_B
  - Output C
  - COM

  - **ULN2003A**: R_B = 2.7 kΩ
  - **ULN2004A**: R_B = 10.5 kΩ

All resistor values shown are nominal.

**absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

- Collector-emitter voltage: 50 V
- Input voltage, V_I (see Note 1): 30 V
- Peak collector current (see Figures 14 and 15): 500 mA
- Output clamp current, I_OK: 500 mA
- Total emitter-terminal current: -2.5 A
- Continuous total power dissipation: See Dissipation Rating Table
- Operating free-air temperature range, T_A: -20°C to 85°C
- Storage temperature range, T_stg: -65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: 260°C

**NOTE 1**: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

**DISSIPATION RATING TABLE**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>T_A = 25°C POWER RATING</th>
<th>DERATING FACTOR ABOVE T_A = 25°C</th>
<th>T_A = 85°C POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>950 mW</td>
<td>7.6 mW/°C</td>
<td>494 mW</td>
</tr>
<tr>
<td>N</td>
<td>1150 mW</td>
<td>9.2 mW/°C</td>
<td>598 mW</td>
</tr>
</tbody>
</table>
### Electrical Characteristics, $T_A = 25^\circ C$ (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST FIGURE</th>
<th>TEST CONDITIONS</th>
<th>ULN2001A</th>
<th>ULN2002A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I(\text{on})$ On-state input voltage</td>
<td>6</td>
<td>$V_{CE} = 2 V, I_C = 300 mA$</td>
<td>13</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{CE\text{sat}}$ Collector-emitter saturation voltage</td>
<td>5</td>
<td>$I_I = 250 \mu A, I_C = 100 mA$</td>
<td>0.9</td>
<td>1.1</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_I = 350 \mu A, I_C = 200 mA$</td>
<td>1</td>
<td>1.3</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_I = 500 \mu A, I_C = 350 mA$</td>
<td>1.2</td>
<td>1.6</td>
<td>1.2</td>
</tr>
<tr>
<td>$V_F$ Clamp forward voltage</td>
<td>8</td>
<td>$I_F = 350 mA$</td>
<td>1.7</td>
<td>2</td>
<td>1.7</td>
</tr>
<tr>
<td>$I_CEX$ Collector cutoff current</td>
<td>1</td>
<td>$V_{CE} = 50 V, I_I = 0$</td>
<td>50</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>$V_{CE} = 50 V, I_I = 0, T_A = 70^\circ C, V_I = 6 V$</td>
<td>100</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>$I_I(\text{off})$ Off-state input current</td>
<td>3</td>
<td>$V_{CE} = 50 V, I_C = 500 \mu A, T_A = 70^\circ C$</td>
<td>50</td>
<td>65</td>
<td>50</td>
</tr>
<tr>
<td>$I_I$ Input current</td>
<td>4</td>
<td>$V_I = 17 V$</td>
<td>0.82</td>
<td>1.25</td>
<td>mA</td>
</tr>
<tr>
<td>$I_R$ Clamp reverse current</td>
<td>7</td>
<td>$V_R = 50 V, T_A = 70^\circ C$</td>
<td>100</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_R = 50 V$</td>
<td>50</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td>$h_{FE}$ Static forward current transfer ratio</td>
<td>5</td>
<td>$V_{CE} = 2 V, I_C = 350 mA$</td>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_I$ Input capacitance</td>
<td></td>
<td>$V_I = 0, f = 1 MHz$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST FIGURE</th>
<th>TEST CONDITIONS</th>
<th>ULN2003A</th>
<th>ULN2004A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I(\text{on})$ On-state input voltage</td>
<td>6</td>
<td>$V_{CE} = 2 V$</td>
<td>5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 125 mA$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 200 mA$</td>
<td>2.4</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 250 mA$</td>
<td>2.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 275 mA$</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 300 mA$</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_C = 350 mA$</td>
<td>8</td>
<td></td>
<td></td>
</tr>
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<td>$V_{CE\text{sat}}$ Collector-emitter saturation voltage</td>
<td>5</td>
<td>$I_I = 250 \mu A, I_C = 100 mA$</td>
<td>0.9</td>
<td>1.1</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_I = 350 \mu A, I_C = 200 mA$</td>
<td>1</td>
<td>1.3</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_I = 500 \mu A, I_C = 350 mA$</td>
<td>1.2</td>
<td>1.6</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_CEX$ Collector cutoff current</td>
<td>1</td>
<td>$V_{CE} = 50 V, I_I = 0$</td>
<td>50</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>$V_{CE} = 50 V, T_A = 70^\circ C, V_I = 1 V$</td>
<td>100</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>$V_F$ Clamp forward voltage</td>
<td>8</td>
<td>$I_F = 350 mA$</td>
<td>1.7</td>
<td>2</td>
<td>1.7</td>
</tr>
<tr>
<td>$I_I(\text{off})$ Off-state input current</td>
<td>3</td>
<td>$V_{CE} = 50 V, I_C = 500 \mu A, T_A = 70^\circ C$</td>
<td>50</td>
<td>65</td>
<td>50</td>
</tr>
<tr>
<td>$I_I$ Input current</td>
<td>4</td>
<td>$V_I = 3.85 V$</td>
<td>0.93</td>
<td>1.35</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = 5 V$</td>
<td>0.35</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_I = 12 V$</td>
<td>1</td>
<td>1.45</td>
<td></td>
</tr>
<tr>
<td>$I_R$ Clamp reverse current</td>
<td>7</td>
<td>$V_R = 50 V$</td>
<td>50</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_R = 50 V, T_A = 70^\circ C$</td>
<td>100</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>$C_I$ Input capacitance</td>
<td></td>
<td>$V_I = 0, f = 1 MHz$</td>
<td>15</td>
<td>25</td>
<td>15</td>
</tr>
</tbody>
</table>

**Post Office Box 655303 • Dallas, Texas 75265**
switching characteristics, $T_A = 25^\circ C$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$ Propagation delay time, low-to-high-level output</td>
<td>See Figure 9</td>
<td>0.25</td>
<td>1</td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$t_{PHL}$ Propagation delay time, high-to-low-level output</td>
<td>$V_S = 50 , V, , I_O \approx 300 , mA$</td>
<td>0.25</td>
<td>1</td>
<td></td>
<td>$\mu s$</td>
</tr>
<tr>
<td>$V_{OH}$ High-level output voltage after switching</td>
<td>$V_S - 20$ V</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

PARAMETER MEASUREMENT INFORMATION

Figure 1. $I_{CEX}$ Test Circuit

Figure 2. $I_{CEX}$ Test Circuit

Figure 3. $I_{I(off)}$ Test Circuit

Figure 4. $I_I$ Test Circuit

Figure 5. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

Figure 6. $V_{I(on)}$ Test Circuit

NOTE: $I_I$ is fixed for measuring $V_{CE(sat)}$, variable for measuring $h_{FE}$. 
PARAMETER MEASUREMENT INFORMATION

Figure 7. $I_R$ Test Circuit

Figure 8. $V_F$ Test Circuit

VOLTAGE WAVEFORMS

Figure 9. Propagation Delay Time Waveforms

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

NOTES:
A. The pulse generator has the following characteristics: $PRR = 12.5 \text{ kHz}$, $Z_O = 50 \Omega$.
B. $C_L$ includes probe and jig capacitance.
C. For testing the ULN2001A and the ULN2003A, $V_{IH} = 3 \text{ V}$; for the ULN2002A, $V_{IH} = 13 \text{ V}$; for the ULN2004A, $V_{IH} = 8 \text{ V}$.
TYPICAL CHARACTERISTICS

**COLLECTOR-EMITTER SATURATION VOLTAGE**

**vs**

**COLLECTOR CURRENT**

(TWO DARLINGTONS PARALLELED)

**COLLECTOR-EMITTER SATURATION VOLTAGE**

**vs**

**TOTAL COLLECTOR CURRENT**

(TWO DARLINGTONS PARALLELED)

**COLLECTOR CURRENT**

**vs**

**INPUT CURRENT**

---

**Figure 11**

**Figure 12**

**Figure 13**
D PACKAGE
MAXIMUM COLLECTOR CURRENT

vs
DUTY CYCLE

N = Number of Outputs Conducting Simultaneously

T_A = 70°C

N = 6
N = 5
N = 7

IC – Maximum Collector Current – mA

V
100
200
300
400
500
600

0 10 20 30 40 50 60 70 80 90 100

Duty Cycle – %

Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT

vs
DUTY CYCLE

N = Number of Outputs Conducting Simultaneously

T_A = 85°C

N = 5
N = 6
N = 7

IC – Maximum Collector Current – mA

V
100
200
300
400
500
600

0 10 20 30 40 50 60 70 80 90 100

Duty Cycle – %

Figure 15
APPLICATION INFORMATION

Figure 16. P-MOS to Load

Figure 17. TTL to Load

Figure 18. Buffer for Higher Current Loads

Figure 19. Use of Pullup Resistors to Increase Drive Current
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